UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,637	09/29/2004	Huajie Chen	FIS920040070	5636

32074 7590 01/25/2006

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER
CHIU, TSZ K

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/711,637	CHEN ET AL.
	Examiner	Art Unit
	Tsz K. Chiu	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *15-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-14* is/are rejected.

7)☒ Claim(s) *6-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group I, claims 1-14 in the reply filed on January 6, 2006 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-5, and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (6,136,636) in view of Chen et al. (6,891,192).

With respect to claim 1-3, Wu discloses a gate stack (8, 28, For example Fig. 11) overlying a single-crystal semiconductor region of a substrate consists essentially of silicon (2, For example Fig. 11), said single-crystal semiconductor region having a first composition, a pair of first spacers (14, For example Fig. 11) disposed over opposite sidewalls of said gate stack (8,28, For example Fig. 11), a pair of a source and drain region (20a, For example Fig. 11) at least partly disposed in respective ones of said semiconductor alloy regions (2, For example Fig. 11), said source and said drain region (20a, For example Fig. 11) each spaced a second distance from said gate stack by a first spacer (14, For example Fig. 11) of said pair of first spacers.

However, Wu did not disclose a pair of regions consisting essentially of a single-crystal semiconductor alloy having a second composition different from said first composition, said semiconductor alloy regions disposed on opposite sides of said gate stack, each said semiconductor alloy region spaced a first distance from said gate stack and said second distance being different from the first distance.

Chen discloses a semiconductor alloy regions are at least partly disposed in trenches disposed in said single-crystal semiconductor regions (21, For example Fig. 1) consisting essentially of a single-crystal semiconductor alloy (14, For example Fig. 1) having a second composition different from said first composition (18, For example Fig. 1), said semiconductor alloy regions consist essentially of silicon germanium (14, For example Fig. 1) disposed on opposite sides of said gate stack (10, For example Fig. 1), each said semiconductor alloy region spaced a first distance from said gate stack, and second distance is longer than said first distance.

Since Wu and Chen are both from the same field of endeavor fabrication of semiconductor integrated circuits, the purpose disclosed by Chen would have been recognized in the pertinent art of Wu.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have use Chen Silicon-germanium region under the source/drain region for the purpose of create a compressive strain to increase hole mobility in the channel region of a PFET by growing an epitaxial layer of Si-Ge in the source and drain regions of the PFET.

With respect to claim 5, Wu discloses the invention set forth to claim 1, but did not disclose substrate is a silicon-on-insulator (SOI) substrate and said single silicon-crystal silicon region is disposed above a buried oxide layer of said SOI substrate.

Chen discloses substrate is a silicon-on-insulator (SOI) substrate and said single silicon-crystal silicon region is disposed above a buried oxide layer of said SOI substrate (column 2, lines 57-61).

Since Wu and Chen are both from the same field of endeavor fabrication of semiconductor integrated circuits, the purpose disclosed by Chen would have been recognized in the pertinent art of Wu.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have use Chen SOI substrate in to Wu invention for the reason that SOI can prevent pass-gate leak and used to reduce stray capacitance for high-speed and or low-power CMOS and may also be used for high voltage applications.

With respect to claim 8-9, Wu discloses an extension and halo regions (20b, For example Fig. 11) underlying said first spacers (14, For example Fig. 11) and at least partly underlying said gate stack (8, For example Fig. 11).

With respect to claim 10, Wu discloses sidewalls of said gate stack are oxidized (12, For example Fig. 11), where in said first spacers (14, For example Fig. 11) are disposed over said oxidized sidewalls (12, For example Fig. 11)

With respect to claim 11, Wu discloses forming second spacers (26, For example Fig. 11) disposed laterally outward from said first spacers (14, For example Fig. 11).

With respect to claim 12, Wu discloses silicide regions (28, 30, For example Fig. 11) overlying said silicon germanium regions, said silicide regions (28, For example Fig. 11) spaced from said gate stack by said first spacers (14, For example Fig. 11) and said second spacers (26, For example Fig. 11).

With respect to claim 13, Wu discloses gate stack (8, 28, For example Fig. 11) includes a gate silicide region (28, For example Fig. 11) and a polycrystalline semiconductor region (8, For example Fig. 11), said gate silicide region overlying and self-aligned to said polycrystalline semiconductor region.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (6,891,192).

With respect to claim 14, Chen discloses a gate stack (10, For example Fig. 1) overlying a single-crystal silicon region of a silicon-on-insulator (column 2, lines 57-61) substrate (16, For example Fig. 1), a pair of first spacers (30, For example Fig. 1) disposed over opposite sidewalls of said gate stack, a pair of regions consisting

essentially of single-crystal silicon germanium (21, 24, For example Fig. 1) disposed on opposite sides of said gate stack, each said silicon germanium region spaced a first distance from said gate stack, a pair of a source region and a drain region (22,46, For example Fig. 1) at least partly disposed in respective ones of said silicon germanium regions (21,24, For example Fig. 1), said source region and drain region each spaced a second distance from spacer of said pair of spacers, and silicide regions, at least one of said silicide regions (28, For example Fig. 1) disposed as a layer of said gate stack, and at least one of said silicide regions (24, For example Fig. 1) at least partly overlying said silicon germanium regions (21, For example Fig. 1).

Allowable Subject Matter

Claim 6-7, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The cited art of record fails to teach wherein said silicon germanium regions have bottom edges disposed at a depth of about 80% to 90% of a depth of a top of said buried oxide layer from a top surface of said single- crystal silicon region.

Claim 6-7, would be allowable if rewritten or amended.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 517-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKC
January 20, 2006

Zandra V. Smith
Supervisory Patent Examiner
23 Jan. 2006